WHAT IS CLAIMED IS:

1. A semiconductor memory circuit comprising:

a memory cell that includes

a first capacitor for storing therein electric charge corresponding to stored data, and

a first transistor whose gate is connected to a word line and one of whose source and drain is connected to a first bit line, while the other of whose source and drain is connected to the first capacitor;

a dummy cell that includes

a second capacitor having smaller capacitance than the first capacitor,

a second transistor whose gate is connected to a dummy word line, and one of whose source and drain is connected to a second bit line, while the other of whose source and drain is connected to the second capacitor, and

a third transistor for electrically connecting the second capacitor with a voltage line in accordance with a precharge signal when the dummy word line is inactive, the voltage line supplying a first voltage;

a precharge circuit for precharging the first and second bit lines to a second voltage when the word line and the dummy word line are inactive; and

a sense amplifier for detecting a potential difference caused between the first and second bit lines when the word line and the dummy word line are activated to electrically connect the first and second capacitors to the first and second bit lines, respectively, and for amplifying the voltages of the first and second bit lines either to the first voltage and to the second voltage, or to the second voltage and to the first voltage, respectively,

wherein the transitions of the word line and the dummy word line from the inactivation voltage level to the activation voltage level are both in a direction from the

second voltage to the first voltage.

2. The semiconductor memory circuit of Claim 1, wherein the capacitance of the second capacitor is substantially half of the capacitance of the first capacitor.

3. The semiconductor memory circuit of Claim 2, wherein
the first and second capacitors are both stacked capacitors, and
the first capacitor is formed to have HSG structure.

4. The semiconductor memory circuit of Claim 2, wherein
the first capacitor is a stacked capacitor, and
the second capacitor is a planar capacitor.

5. The semiconductor memory circuit of Claim 2, wherein
the first capacitor is a trench capacitor, and
the second capacitor is a planar capacitor.

6. The semiconductor memory circuit of Claim 1, wherein the amplitude of the dummy word line voltage is smaller than the amplitude of the word line voltage.

7. A semiconductor memory circuit comprising:
a memory cell that includes
a first capacitor for storing therein electric charge corresponding to stored data, and
a first transistor whose gate is connected to a word line and one of whose

source and drain is connected to a first bit line, while the other of whose source and drain is connected to the first capacitor;

a dummy cell that includes

a second capacitor,

a second transistor whose gate is connected to a dummy word line, and one of whose source and drain is connected to a second bit line, while the other of whose source and drain is connected to the second capacitor, and

a third transistor for electrically connecting the second capacitor with a voltage line in accordance with a precharge signal when the dummy word line is inactive, the voltage line supplying a first voltage;

a precharge circuit for precharging the first and second bit lines to a second voltage when the word line and the dummy word line are inactive; and

a sense amplifier for detecting a potential difference caused between the first and second bit lines when the word line and the dummy word line are activated to electrically connect the first and second capacitors to the first and second bit lines, respectively, and for amplifying the voltages of the first and second bit lines either to the second voltage and to a third voltage, or to the third voltage and to the second voltage, respectively,

wherein the transitions of the word line and the dummy word line from the inactivation voltage level to the activation voltage level are both in a direction from the second voltage to the third voltage; and

the amplitude of the dummy word line voltage is smaller than the amplitude of the world line voltage.

8. The semiconductor memory circuit of Claim 7, wherein

the capacitance of the second capacitor is substantially equal to the capacitance of

the first capacitor, and

the first voltage is an intermediate voltage between the second and third voltages.

9. The semiconductor memory circuit of Claim 7, wherein

the first and second transistors are NMOS transistors, and

the inactivation voltage of the dummy word line is higher than the inactivation voltage of the word line.

10. The semiconductor memory circuit of Claim 9, wherein

the inactivation voltage of the word line is lower than the second voltage, and

the inactivation voltage of the dummy word line is substantially equal to the second voltage.

11. The semiconductor memory circuit of Claim 7, wherein

the first and second transistors are PMOS transistors, and

the inactivation voltage of the dummy word line is lower than the inactivation voltage of the word line.

12. The semiconductor memory circuit of Claim 11, wherein

the inactivation voltage of the word line is higher than the second voltage, and

the inactivation voltage of the dummy word line is substantially equal to the second voltage.

13. The semiconductor memory circuit of Claim 1, wherein the second and third transistors are disposed substantially on a straight line with the second capacitor being

interposed between the second and third transistors.

14. The semiconductor memory circuit of Claim 13, wherein the first and second capacitors are both planar capacitors.

15. The semiconductor memory circuit of Claim 7, wherein the second and third transistors are disposed substantially on a straight line with the second capacitor being interposed between the second and third transistors.

16. The semiconductor memory circuit of Claim 15, wherein the first and second capacitors are both planar capacitors.